White paper

Fast Switching Power Delivery Architecture and Load-Aware DVFS

In today's world of ubiquitous computing driven by data and power-hungry applications, power management is at the forefront of system, network, and software challenges. Smart devices, edge computing and cloud processing all have unique requirements for efficient power delivery to achieve low latency and high throughput at aggressive product cost and energy consumption targets.

To meet these demands, power management solutions must provide ultra-fast energy delivery that can be system-CONTROLLED to meet overall power needs with ever-shrinking footprints. Integration and coupling of power management and computing platforms are essential to keep pace with continuing improvements in speed, efficiency, cost, and size.

Here Endura Technologies discusses its technology and approach to meet these demanding needs.

Today, many Power Management Integrated Circuits (PMICs) are based on the DC-DC Converter, a 30+ year old architecture. To meet modern demands, the DC-DC converter must achieve near-perfect efficiency: change regulated voltage almost instantaneously, maintain load regulation under stringent transients, and switch at higher speeds to reduce passive components form factors. This is a challenge for the industry.

The answer is a combination of architecture, system, and semiconductor solutions.

Historically PMICs have used legacy process nodes and associated Bipolar CMOS DMOS (BCD) variants. Foundries are now providing high voltage capabilities on advanced process nodes allowing for faster switching speeds with minimal efficiency deltas. This is a key element for defining new architectures.

Endura Technologies' new power delivery architecture, Bypass Dual Duty Cycle control (BDDC™), provides the following advanced features:

- Unconditionally stable control for fast switching and Dynamic Voltage Control (DVC)
- Flat efficiency via seamless transitions from Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).
- Stable operation at high switching frequencies with no reliance on current sensing or zero crossing comparator; maximum frequency is set by the process and switching losses.
- Fast digital load current monitoring which provides:
    - Digital Leg and Phase Shedding
    - Proprietary Load-Aware DVFS (LA-DVFS™)

Bypass Dual Duty Cycle Control Technology (BDDC)

Referencing Figure 1, two independent Pulse Width Modulation (PWM) Generators produce duty cycles of PWM_{base} and PWM_{adj}.

Under light load conditions, only PWM_{base} is used to keep the device in DCM mode. When V_{out} drops below tolerance, a PWM pulse is generated to switch on the Power Stages and regulate the output. Otherwise, no current is sent to C_{out} until the load needs to be increased.

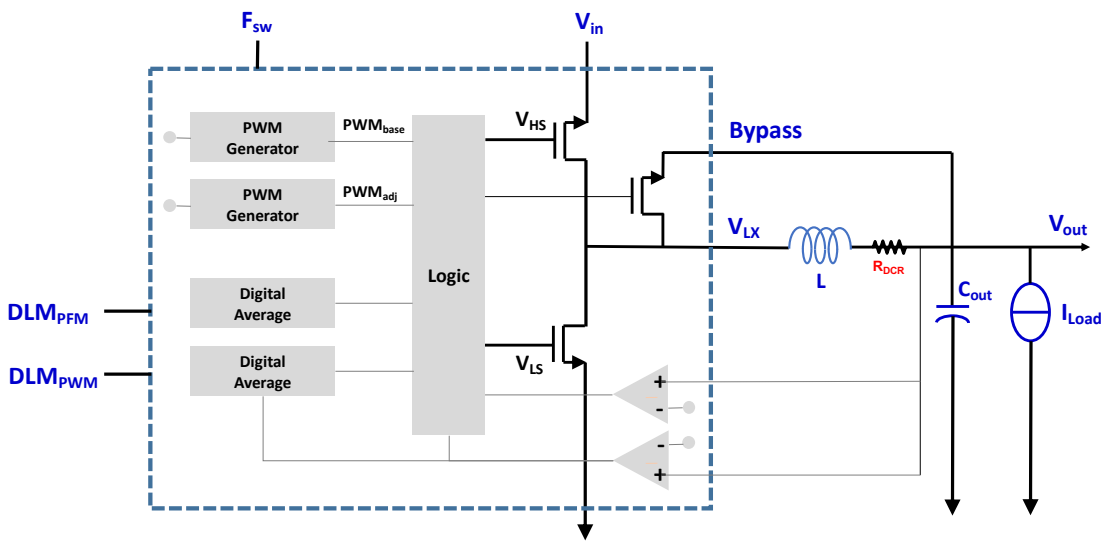

Figure 1: Simplified Bypass Dual Duty Cycle Control (BDDC) Architecture

In DCM, Pulse Frequency Modulation (PFM) operation is used. As the load increases, PFM becomes continuous, and the Output seamlessly transitions to CCM and PWM operation, as shown in Figure 2.

In CCM, the system oscillates between PWM_{base} and PWM_{adj} where PWM_{adj} is set to ensure proper regulation at maximum load.

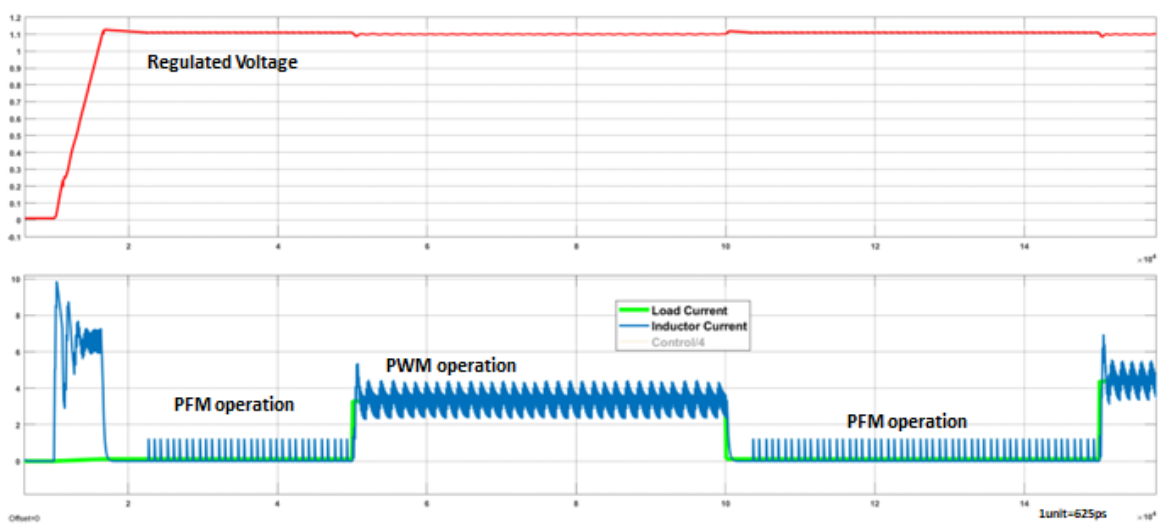

Figure 2: BDDC™ Start-up and Load Transient Regulation

Bypass Mode

Bypass Mode is only active in DCM and CCM overshoot conditions.

In CCM with an overshoot above tolerance, the device automatically enters DCM, and the internal Bypass Switch shorts the external inductor (L); the inductor then dissipates its current in a free-wheeling loop. No additional current is sourced to the load.

The benefits of Bypass Mode are:

- Eliminates ringing in DCM
- Prevents overshoot with high-to-low load transients
- Enables DVC ramping of V_{out} at the highest slew rate without ringing; see Figure 3

This Bypass Switch also eliminates resonances, which allows the system to operate at high speed and be unconditionally stable.

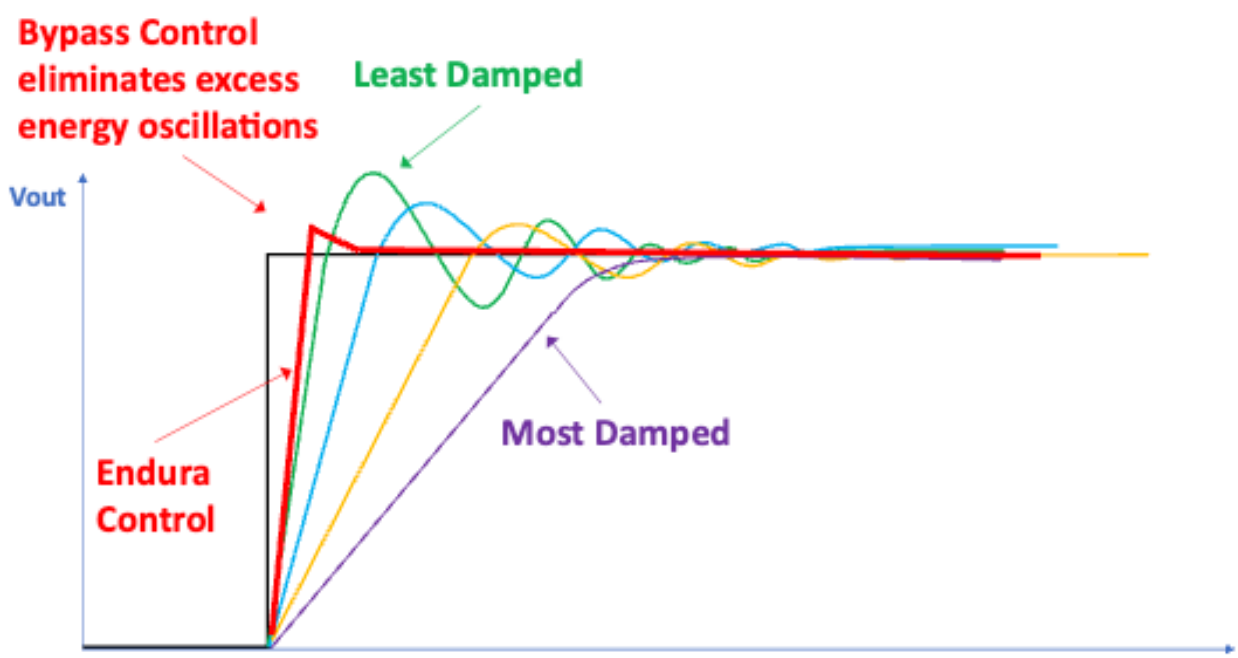

Figure 3: BDDC Bypass Mode Minimizes Ringing With Fast Slew Rates

Seamless PFM-PWM Transition

Per Figure 2, in light load conditions, DCM (PFM mode) will automatically transition to CCM (PWM mode) as the load increases. Conversely, as the load decreases to a set point, the Bypass Switch will automatically engage and transition to DCM with PFM pulses regulating light load conditions until the load increases and automatically transitions to CCM.

Traditional approaches rely on current monitoring to switch between PFM and PWM modes and require hysteresis to reduce the effect of inaccuracy and latency causing efficiency discontinuities.

BDDC does not need current sensing or zero crossings which allows seamless PFM-PWM operation at the maximum switching speed based on the process node. As shown in Figure 4, efficiency remains flat over a broad load current range during the PFM-PDM transitions.

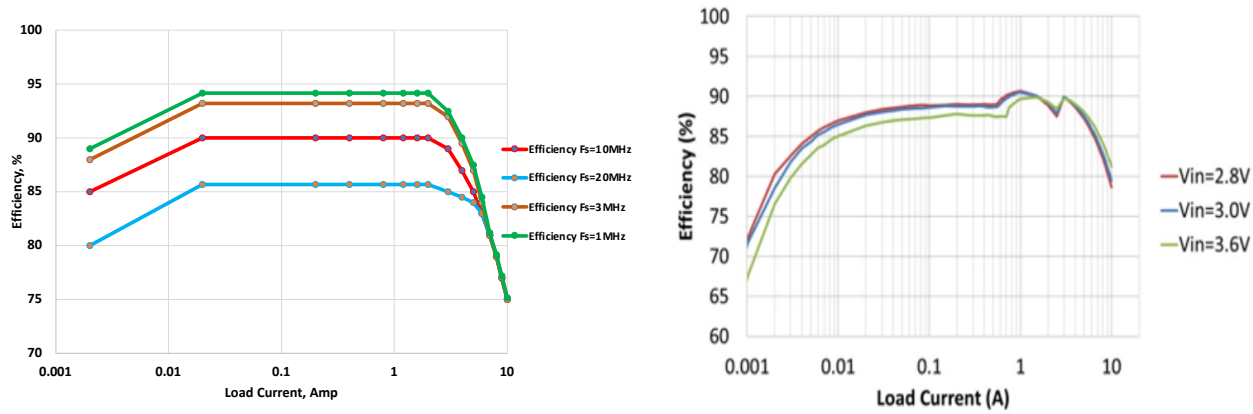

Figure 4: Flat Efficiency Over Broad Load Current Range (Dual-Phase Shown, V_{in}=3.6V) vs. Competition (F_{sw}=3MHz)

AC Regulation in Extreme Transients

To mitigate sub-harmonic ripple on V_{out}, a proprietary AC Regulation was developed to keep the ripple within the milli-volt range and does not affect the unconditional stability of the system.

This AC Regulation protects against droop and overshoot with load transients. Figure 5 shows a Single-Phase Buck regulated under varying load transient at a high slew rate.

Seamless PFM-to-PWM operation is maintained throughout.

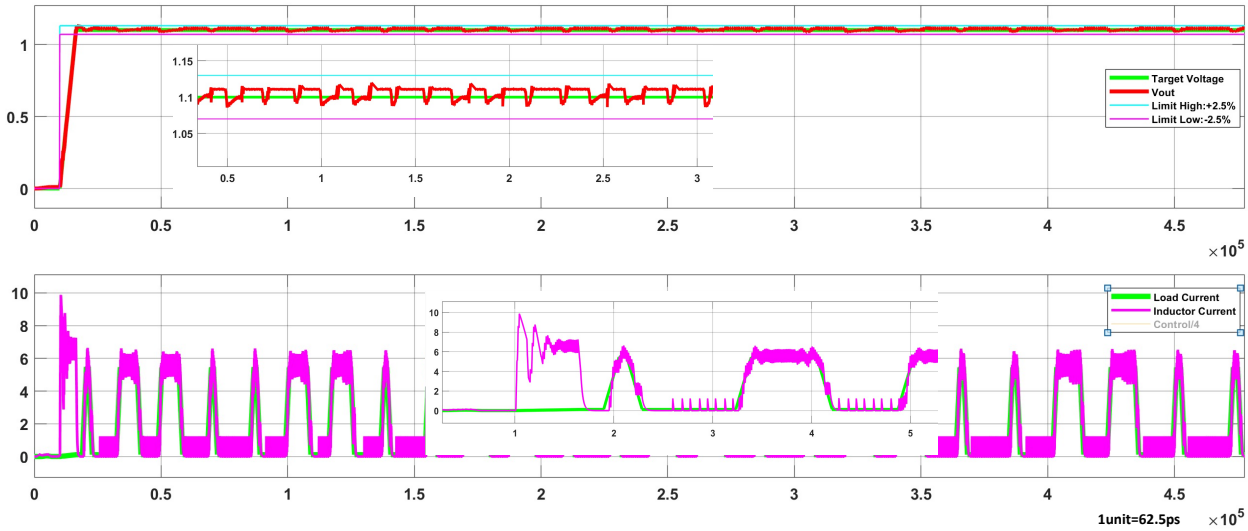

Figure 5: AC Regulation within +/- 2.5%; F_s=10MHz, L=60nH, C_{out}=20uF, Single Phase BDDC with 0-to-5A pseudo random transients at 7A/us. Device ramps from 0 to 1.1V in 4us. It transitions seamlessly from PFM to PWM mode and vice versa

Digital Load Monitoring (DLM)

In CCM, the duty cycle between PWM_{adj} and PWM_{base} is linearly dependent on load current. Averaging the comparator bitstream provides an accurate digital signature of the load current as shown in Figure 6.

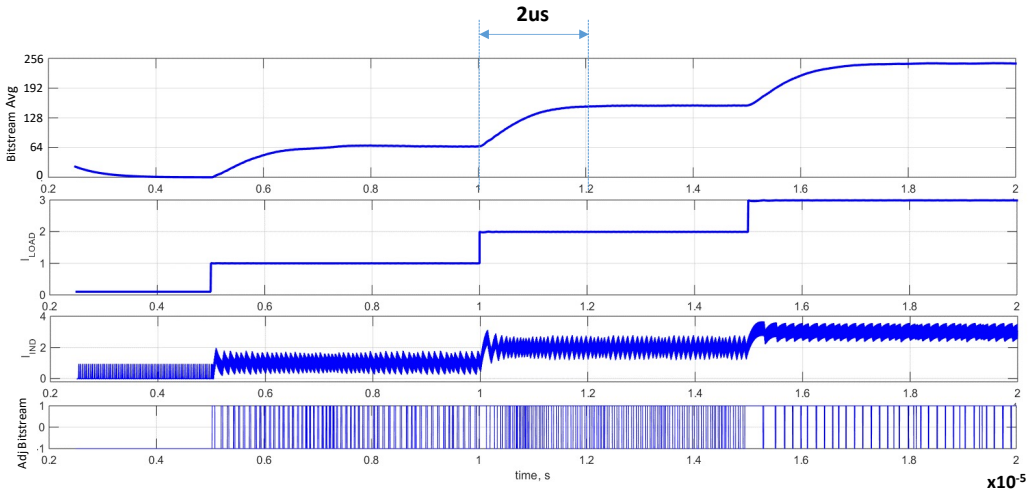

Figure 6: Fs=20MHz, L=36nH, C_{out}=10uF, Single Phase BDDC Reporting Current Steps in <2us

When not adjusting, the 8-bit comparator's average output is zero signaling the device is in light load. When the system is constantly adjusting, the comparator's average output is 256 bits signaling the load is at the maximum current that can be regulated.

In DCM (PFM), the density of current pulses is proportional to the load current. Similarly, averaging the bypass comparator output provides the digital signature of the light load current.

DLM allows for effective Digital Leg and Phase Shedding in multi-phase operation. Used in combination with Endura Technologies' AC Regulation, it achieves artifact-free leg and phase shedding while increasing efficiency and extending load range.

Next, we discuss how rapid DLM can be used to significantly improve system efficiency with companion SoC's using Load-Aware Dynamic Voltage Frequency Scaling (LA-DVFS™).

Load-Aware DVFS Operation

Modern computing devices/systems consume energy as a function of applications that dynamically drive data transfer and computational demands. These varying loads must be addressed with low latency to improve performance and reduce energy consumption.

Dynamically adjusting digital clock frequencies and supply voltages is not new. The opportunity is reducing response latency so that energy is sourced only as needed; this translates into fast DVC.

With DLM providing the digital load signature in real-time, the system is also made "load aware" in real-time. This speeds up the ability to adjust frequency and voltage within the system with hardware and/or software.

Part of the power delivery architecture is that BDDC technology can operate DC-DC conversions at very high switching speeds. Endura Technologies has demonstrated a multi-phase embedded voltage regulator

(eVR) at 150MHz (1V supply). Endura Technologies has also demonstrated a 5V DC-DC converter at 20MHz with DLM of <2us latency. This enables micro-second (potentially less) hardware-based LA-DVFS in a system while also enabling extremely fast software-based LA-DVFS depending on the operating system.